## REMARKS

By this amendment claim 5 has been canceled, claims 1-4, 6-7 and 17 have been amended and claims 28-32 have been added. Claims 1-4, 6-19 and 24-32 are pending. Reconsideration of the application as amended is respectfully requested.

### Rejections under 35 USC §102(e)

Claims 1, 2, 8, 11, 15, and 17 have been rejected under 35 USC §102(e) over Saito et al. (US Pub. 2002/0020058).

Saito at FIG. 6 depicts a ball grid array (BGA) body 4 having first and second BGA-side pads 5. FIG. 10 of Saito depicts the BGA body 4 comprising a silicon chip 20 (i.e. a wafer section), the chip 20 presumably comprising bond pads (not depicted) connected with BGA substrate (not numbered) using bond wires (not numbered) and encapsulated in BGA material (not numbered), typically referred to as "glob top". The BGA-side pads 5 are presumably electrically separated. Saito further depicts a printed circuit board (PCB) having first and second through-hole upper lands 1. Each BGA-side pad 5 is electrically coupled with one of the through-hole upper lands 1 using solder 6 and solder paste 3.

Claim 1 recites the steps of "forming a semiconductor wafer section comprising first, second, and third pads thereon which are electrically separated from each other" forming first, second, and third circuit portions, each respectively electrically coupled with the first, second, and third pads, "selectively electrically connecting together either said first and second pads or said second and third pads to electrically connect either said first and second circuit portions or said second and third circuit portions, wherein said wafer section is enabled to function with a first operational mode if said first and second pads are electrically connected together, and is enabled to function with a second operational mode different from said first operational mode if said second and third pads are electrically connected together."

Claim 1 recites novel and nonobvious differences over the disclosure of Saito. Saito does not teach or suggest the selective connection of first and second pads or second and third pads to enable a wafer section to function with a first or second operational mode. Saito at FIG. 9 discusses the accidental electrical connection of two ball bonds together if an excessive amount of solder is placed within the through-holes. However, Saito teaches that this is to be avoided, and this undesirable bridging is not selectively performed to result in one of two operational modes. Further, element 7 of Saito is not a "semiconductor wafer section" but is instead a printed circuit board. Saito teaches a semiconductor die 20, for example at FIG. 10, which is encapsulated in material 4 of FIG. 10 prior to performing the teachings of Saito.

Claim 2 recites "attaching a single ball bond to two of said pads." Saito does not teach or suggest attaching a single ball bond to two of the pads, and thus claim 2 is further allowable over Saito under 35 USC §102(e)

Rejected claim 8 is allowable under 35 USC §102(e) over Saito as applied by the Examiner, as it is not evident where various elements of the claims are taught by Saito, and the Examiner has not indicated what is being relied upon to teach the recitations of the rejected claims. It is further submitted that because the elements the Examiner is relying upon to teach the claimed features has not been pointed out, the applicant has not been given fair opportunity to reply to the Examiner's rejection.

For example, claim 8 is allowable under 35 USC §102(e) over Saito, at least because it appears that Saito fails to teach or suggest "providing a transistor electrically coupled with said first conductive pad portion." Saito also fails to teach or suggest "providing one of a fuse array and an antifuse array...electrically coupled with said second conductive pad portion." Saito also fails to teach or suggest "electrically coupling said second pad portion to a voltage source" and also "with said second pad portion electrically coupled to said voltage source, programming said array" and also "subsequent to programming said array, electrically coupling said first pad portion with said second pad portion." Any one of these elements alone, if not taught or suggested by Saito, is sufficient to render claim 8 allowable over Saito under 35 USC §102(e). The Examiner has not indicated where Saito supposedly teaches these claimed elements.

Claim 11 is also allowable over Saito, as Saito does not appear to teach or suggest "providing a bond pad comprising at least three separate sections electrically isolated from each other," "providing at least three circuit portions with one circuit portion electrically connected with only one of said bond pad portions" and "electrically interconnecting said at least three bond pad sections to electrically connect said at least three circuit portions." While it is conceded that Saito may have three or more BGA pads 5 or through-hole upper lands 1, these are three separate pads and not three separate sections of a bond pad. Also, Saito does not appear to teach or suggest electrically interconnecting at least three bond pad sections to electrically connect the three circuit portions.

Claim 15 is also allowable over Saito. The physical arrangement of Saito requires that only a single pad 5 on body 4 can be connected with a land 1 on PCB 7. Thus there is no freedom is selecting from more than one pad 5 to connect with a land 1. Thus it does not appear possible with the invention of Saito as applied by the Examiner to "select an operation mode of said semiconductor device by selectively connecting at least two of said plurality of conductive pads to each other to selectively connect at least two of said plurality of circuits." It is beyond the scope of Saito to selectively connect a pad with a land, as each pad must necessarily be connected to the pad it is aligned with and which it directly overlies.

Claim 17 is allowable over Saito as Saito fails to teach or suggest "forming first and second spaced conductive pads on said semiconductor wafer section; and forming first and second internal power buses on said wafer section...wherein said first and second conductive pads are adapted to be electrically coupled to each other to electrically connect said first power bus with said second power bus." Saito does not teach or suggest that two pads formed on wafer section 4 are adapted to be electrically coupled to each other to electrically connect the first power bus with the second power bus.

Thus it is submitted that rejected claims 1, 2, 8, 11, 15, and 17 are allowable over Saito under 35 USC §102(e).

**Rejections under 35 USC §103(a)**

Remaining claims 3, 4, 6, 7, 9-10, 12-14, 16, 18-19, and 24-27 have been rejected under 35 USC §103(a) over Saito et al. in view of Johnston (US 5,898,217) and admitted prior art. Saito discloses the BGA device comprising an internal die as described relative to the rejections under 35 USC §102(e). Johnston describes the connection of a semiconductor die 110 (i.e. a semiconductor wafer section) to a substrate 120 (column 2 lines 53-55). The substrate 120 is manufactured from multiple ceramic layers, with printed wires 128a running between the layers of ceramic (column 3 lines 20-25 and 47-50).

In re claims 3-4 and 14, the Examiner combines the printed wire within the ceramic substrate of Johnston to teach the wire bond of the present claims. The Examiner states that element 128a of FIG. 2 of Johnston is a "wire bond." However, element 128a is not a "wire bond" as known in the art, but is instead a printed wire formed during the manufacture of the substrate 120, and within the ceramic layer structure. Such a structure is not a "wire bond." Johnston does, in fact, recite the use of a wire bond, but as a functional equivalent to solder bumps 113 which would connect the die with pads 121 directly. Further, Saito also appears to teach wire bonds in FIG. 10, for example, to connect the die with the BGA body substrate. Also, the Examiner uses solder bump 113 as suggests that this teaches "screen printing a conductive epoxy to the first and second bond pad portions"

Saito and Johnston in combination fail to teach or suggest the invention as recited in rejected claims 3 and 4. Neither Saito nor Johnston recites the limitations of claim 1 from which claims 3 and 4 depend of "forming a semiconductor wafer section comprising first, second, and third pads thereon which are electrically separated from each other" forming first, second, and third circuit portions, each respectively electrically coupled with the first, second, and third pads, "selectively electrically connecting together either said first and second pads or said second and third pads to electrically connect either said first and second circuit portions or said second and third circuit portions, wherein said wafer section is enabled to function with a first operational mode if said first and second pads are electrically connected together, and is enabled to function with a second operational mode different from

said first operational mode if said second and third pads are electrically connected together." Johnson provides a wafer section 110 presumably having bond pads, and connecting a bond pad on die 110 to a pad 121, but does not selectively connect first and second pads, or second and third pads, to select an operational mode of the die. Saito also provides a die, but lacks the same teaching, reciting only coupling a pad 5 on the BGA substrate to a land 1 on the PCB 7, and apparently, in FIG. 10, wire bonding a bond pad of die 20 to the BGA substrate (unnumbered). As each reference fails to teach the selective electrical connection of two pads from three pads on a semiconductor wafer section, the references cannot teach doing so with wire bonds as recited in claim 3 or screen printing of epoxy as recited in claim 4. As the references do not teach or suggest all the claim limitations as required (MPEP §706.02(j)), claims 4 and 3 are allowable over Saito and Johnston in combination.

Claim 13 recites "attaching a ball bond to said at least three bond pad sections." Where Saito and Johnston use ball bonds, there is only one ball bond on each pad and there is no suggestion to form a ball bond to at least three separate bond pad sections which are electrically isolated from each other. Thus claim 13 is allowable over Saito and Johnson in combination.

Rejected claims 24-27 recite the formation of a device having a hardwired and selectable CAS latency using a particular method. None of the cited references of Saito, Johnston, or AAPA describe the particular method of selecting a CAS latency by forming a conductor to electrically connect a first pad portion with a second pad portion or forming a conductor to electrically connect the second pad portion with a third pad portion to select a second CAS latency which is different from the first CAS latency. The Examiner has not indicated which is being relied upon to teach the stated method. The rejected claims are therefore allowable over the cited references as applied by the Examiner under 35 USC §103(a).

Saito and AAPA have been combined to reject the invention as recited in claim 6. As discussed above, Saito does not teach or suggest selectively connecting first and second pads to electrically couple one of a fuse and antifuse array to a transistor. As the cited references do not teach or suggest all of the claim limitations, claim 6 is allowable over the cited references under 35 USC §103(a).

AAPA has been cited to teach the lead frame of claims 7 and 12. However, the combination of Saito and Johnston with the lead frame of AAPA would not result in the present invention as claimed. It appears that the lead frame of AAPA would be used in place of the unnumbered substrate of Saito interposed between die 20 and ball bonds 6 in FIG. 10. Thus the die would be wire bonded to the lead frame in accordance with conventional teachings, then the lead frame would be connected to the PCB 7 using ball bonds 6. In any case, as none of the references teach or suggest the process of present claims 1 and 11 as discussed above from which claims 7 and 12 respectively depend, rejected claims 7 and 12 are allowable over the cited references under 35 USC §103(a).

Claim 8 from which claims 9 and 10 depend is allowable over the cited references which fail to teach or suggest providing first and second conductive pad portions electrically isolated from each other, providing a transistor electrically coupled with the first pad portion and a fuse or antifuse array electrically coupled with the second conductive pad portion, electrically coupling the second pad portion to a voltage source, with the second pad portion electrically coupled to the voltage source, programming the array, and subsequent to programming the array, electrically coupling the first pad portion with the second pad portion. The Examiner rejected claim 8 over Saito, however Saito fails to teach or suggest most of the process steps recited in claim 8 as discussed above relative to the rejection of claim 8 under 35 USC §102(e). Thus claims 9 and 10 which depend from claim 8 are allowable over the combination of Saito and AAPA, and further over Johnston under 35 USC §103(a).

Claim 16 is allowable over the cited references, as the references fail to teach or suggest encapsulating the semiconductor wafer section subsequent to the selection of the operational mode. Saito appears to teach the use of a wafer section 20 which is already encapsulated (pointed to by "4" in FIG. 10) prior to the processes the Examiner uses to teach the present invention as claimed. Further, the references do not teach the selection of an operational mode by the stated method regardless of encapsulation, and claim 16 is further allowable over the cited references under 35 USC §103(a).

Claims 18 and 19 recite a particular method using a $V_{SS}$ power bus and a $V_{SSQ}$ power bus. The Examiner states that the two busses and their connection with pads are discussed in ¶¶4-10 of AAPA. However, no reference is made to power busses in the cited paragraphs, and only passing mention is made to power bus configurations in ¶11. Their connection to pads is not discussed except during the disclosure of the invention. It is well established that the teachings of the applicant's own disclosure may not be used as a basis for rejection, and thus any rejection using this disclosure of the present invention as claimed would appear improper. Further, the portion of Saito which the Examiner uses to reject claim 17 from which claims 18 and 19 depend occur after the wafer section 20 is already encapsulated, and thus it does not appear possible to vary connections of an internal power bus using the lands 1 or pads 5 of Saito, which are external to the die 20. Claims 18 and 19 are therefore allowable over the cited references under 35 USC §103(a).

Any claims not individually addresses are allowable at least because they depend from an allowable base claim.

**Conclusion**

If the Examiner believes a conference will expedite prosecution of this case, the Examiner is cordially invited to call the undersigned. This is believed to be a complete and proper response to the Examiner's outstanding restriction requirement.

Respectfully submitted,

Kevin D. Martin
Agent for Applicant
Registration No. 37,882
Micron Technology, Inc.
PO Box 6
Boise, ID 83707-0006
Ph: (208) 368-4516
FAX: (208) 368-5606
e-mail: kmartin@micron.com